PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference TJ0404-PCT	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/JP2004/015179	International filing date *(day/month/year)* 06.10.2004	Priority date *(day/month/year)* 08.10.2003
International Patent Classification (IPC) or national classification and IPC H01L29/78, H01L29/739, H01L29/06, H01L29/423, H01L21/336, H01L21/331		
Applicant TOYOTA JIDOSHA KABUSHIKI KAISHA et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 7 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 8 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☒	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
14.09.2005	03.03.2006
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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/015179

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:

   ☐ international search (under Rules 12.3 and 23.1(b))
   ☐ publication of the international application (under Rule 12.4)
   ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-41	as originally filed
Claims, Numbers	
1-18	received on 14.09.2005 with letter of 12.09.2005
Drawings, Sheets	
1/30-30/30	as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   ☐ the description, pages
   ☐ the claims, Nos.
   ☐ the drawings, sheets/figs
   ☐ the sequence listing *(specify)*:
   ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   ☐ the description, pages
   ☐ the claims, Nos.
   ☐ the drawings, sheets/figs
   ☐ the sequence listing *(specify)*:
   ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/015179

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-18
	No:	Claims	
Inventive step (IS)	Yes:	Claims	2,7,12
	No:	Claims	1,3-6,8-11,13-18
Industrial applicability (IA)	Yes:	Claims	1-18
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Regarding Section V:

1. Reference is made to the following documents:

D1 = US-B-6 194 741

D2 = WO-A-00/70654

D3 = WO-A-99/52152

2. Insofar as the present text can be understood (see Section VIII in this respect), the subject-matter of claims 1, 3-6, 8-11 and 13-18 does not involve an inventive step in the sense of Rule 65(1)-(2) PCT, contrary to the requirements of Article 33(3) PCT:

2.1 D1 (see in particular column 4, lines 49-60 and figure 6) discloses an insulated gate type semiconductor device from which the subject-matter of claim 1 only differs in that (see the body region 23, the drift region 22, the trench section 30, the floating region 32, the insulating layer 31 (being deposited oxide) and the gate electrode 34, a bottom of the trench section being arranged in the floating region, a lower end of the gate electrode being above the top of the floating region and a space between the bottom surface of the body region and the top of the floating region (about 1.4 micrometre as can be estimated) being obviously wider than a space (about 0.2 micrometre as can be estimated) between a lower end of the deposited insulating layer and a lower end of the floating region):

(i) a space between the lower end of the gate electrode and the lower end of the deposited insulating layer is wider than a space between the bottom surface of the body region and the top of the floating region.

However, feature (i) would be routinely determined by the skilled person, eg. by trial and error, in accordance with circumstances, eg. to achieve a different breakdown voltage.
In this respect, it is noted that no unexpected effects or properties would result from

the incorporation of feature (i) in the device of D1, having regard to the content of the present application (see the statements from page 17, line 20 to page 18, line 16, indicating that, essentially, the gate electrode should not face the floating region) and to the teaching of the prior art (see eg. D1, ibid).
Hence, the subject-matter of claim 1 lacks the required inventive step.

2.2 Furthermore, D1 (see column 2, line 36 - column 3, line 50 and figures 1-2) discloses a manufacturing method of an insulated gate type semiconductor device from which the subject-matter of independent claim 11 only differs in that (see the body region 23, the drift region 22, the trench section 30 and the gate electrode 34, the trench forming step carried out after body and drift formation, the impurity injecting (implantation) step into the trench bottom and the subsequent insulating material laying-up step, and the floating region thermal diffusion step):

(ii) an oxide film forming step of forming an oxide film on a side wall of the trench section formed in the trench section forming step is carried out;

(iii) the impurity injecting step is carried out after said oxide forming step;

(iv) the floating region forming step is carried out after the insulating material laying-up step.

However, features (i)-(ii) (to protect the trench during implantation) and (iii) (to anneal the gate insulating material while activating the floating region dopants) are merely normal design options which would be readily considered by the skilled person, where needed.
Hence, the subject-matter of independent claim 11 also lacks the required inventive step.
In this respect it is moreover noted that the device shown in figure 6 of D1 is implicitly manufactured in accordance with the method generally disclosed with respect to the device shown in figures 1-2 of D1.

2.3 The additional features of dependent claims 3 and 6 are merely matters of normal design procedure, see eg. D2, page 7, lines 7-18 and figure 3, and the skilled person

would consider the inclusion of said features in the device known from D1 as constituting obvious design possibilities to increase the breakdown voltage of the device. In this respect it is moreover pointed out that the last feature of dependent claim 6 would be routinely determined by the skilled person, eg. by trial and error, in accordance with circumstances, eg. to achieve a different breakdown voltage.
Furthermore, the additional features of dependent claims 4, 5, 8, 9 and 13 relate to straightforward changes in the subject-matter of dependent claims 3 (regarding claims 4-5 and 9), 6 (regarding claims 8 and 9) or in a manufacturing method corresponding to the subject-matter of claim 3 (regarding claim 13).
Therefore, the subject-matter of dependent claims 3-6, 8, 9 and 13 does not involve an inventive step.

2.4 Providing a termination region having a trench structure with floating regions similar to that of the cell region is a normal design option in the present technical field, see eg. D3, figure 4.
In particular, to simplify manufacturing, the skilled person would readily provide trenches extending into the floating regions in the termination region for a device such as that of D1 having already such trenches in the cell region.
Furthermore, in the finished device the terminal (termination) trench section without gate electrode would be filled with an insulating layer for passivation, as is well-known in the present technical field.
In addition, the last feature of dependent claim 10 would be routinely determined by the skilled person, eg. by trial and error, in accordance with circumstances, to set a desired breakdown voltage.
Hence, the subject-matter of dependent claim 10 does not involve an inventive step either.

2.5 The additional features of dependent claims 14-18 are known from D1 (ibid), at least implicitly.
Therefore, the subject-matter of dependent claims 14-18 does not involve an inventive step either.

3. The subject-matter of claims 1-18 is obviously susceptible of industrial application.

Regarding Section VII:

1. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D3 is not mentioned in the description, nor are these documents identified therein.

2. The features of the claims are not provided with reference signs placed in parentheses, contrary to the requirements of Rule 6.2(b) PCT.

Regarding Section VIII:

The present application does not meet the requirements of Article 6 PCT because claim 1, 14 and 15 are not clear:

1. The wording of device claim 1 leaves a doubt as to the category of said claim since the term "deposited" used in the claim relates to a method of making the device (by deposition as compared with eg. oxidation) rather than imposing any clear restrictions on the device itself.

2. Claims 14 and 15 do not meet the requirements of Article 6 PCT in that the matter for which protection is sought is not clearly defined, the subject-matter of said claims being defined in terms of the result to be achieved although it is possible to define the subject-matter in more concrete terms, namely in terms of how the effect is to be achieved.

CLAIMS

1. (Amended) An insulated gate type semiconductor device comprising:

a body region arranged at upper surface side in a semiconductor substrate, the body region having a first conductive type semiconductor;

a drift region being in contact with bottom surface of the body region, the drift region having a second conductive type semiconductor; and

a trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region,

wherein the insulated gate type semiconductor further comprises a floating region surrounded by the drift region, the floating region having a first conductive type semiconductor,

bottom of the trench section is arranged in the floating region,

in the trench section, there are formed a deposited insulating layer consisting of deposited insulating material and a gate electrode being arranged above the deposited insulating layer and facing the body region, and

a lower end of the gate electrode is further above top of the floating region,

a space between the bottom surface of the body region and the top of the floating region is wider than a space between a lower end of the deposited insulating layer and a lower end of the floating region, and

a space between the lower end of the gate electrode and the lower end of the deposited insulating layer is wider than a space between the bottom surface of the body region and the top of the floating region.

2.(Amended) An insulted gate type semiconductor device according to claim 1 further comprising an intermediate floating region arranged further above top of the floating region with being surrounded by the drift region, the intermediate floating region having a first conductive type semiconductor,

wherein the trench section penetrates the intermediate floating region, and

top of the deposited insulating layer is arranged further above top of the intermediate floating region.

3.(Amended) An insulated gate type semiconductor device according to claim 1 further comprising:

an auxiliary trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region, the auxiliary trench section being filled with insulating material inside; and

an auxiliary floating region surrounded by the drift region, the auxiliary floating region having a first conductive type semiconductor,

wherein bottom of the auxiliary trench section is arranged in the auxiliary floating region.

4.(Unchanged) An insulated gate type semiconductor device according to claim 3 wherein depth of the trench section and depth of the auxiliary trench section are different.

5.(Unchanged) An insulated gate type semiconductor device

according to claim 3 wherein depth of the trench section and depth of the auxiliary trench section are same.

6.(Amended) An insulated gate type semiconductor device comprising:

a body region arranged at upper surface side in a semiconductor substrate, the body region having a first conductive type semiconductor;

a drift region being in contact with bottom surface of the body region, the drift region having a second conductive type semiconductor;

a trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region; and

a gate electrode arranged in the trench section with facing the body region,

wherein the insulated gate type semiconductor device further comprises:

an auxiliary trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region, the auxiliary trench section being filled with insulating material inside; and

an auxiliary floating region surrounded by the drift region, the auxiliary floating region having a first conductive type semiconductor,

wherein bottom of the auxiliary trench section is arranged in the auxiliary floating region, and

a space between the bottom surface of the body region and the top of the auxiliary floating region is wider than a space between

a lower end of the deposited insulating layer and a lower end of the auxiliary floating region.

7. (Amended) An insulated gate type semiconductor device according to claim 6 further comprising an auxiliary intermediate floating region arranged further above top of the auxiliary floating region with being surrounded by the drift region, the auxiliary intermediate floating region having a first conductive type semiconductor,

wherein the auxiliary trench section penetrates the auxiliary intermediate floating region, and

top of the deposited insulating layer is arranged further above top of the auxiliary intermediate floating region.

8. (Amended) An insulated gate type semiconductor device according to claim 6 further comprising:

a second auxiliary trench section facing the auxiliary trench section with the gate electrode inserted between there, the second auxiliary trench section being arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region, the second auxiliary trench section being filled with insulating material inside; and

a second auxiliary floating region surrounded by the drift region, the second auxiliary floating region having a first conductive type semiconductor,

wherein depth of the auxiliary trench section and depth of the second auxiliary trench section are different.

9.(Unchanged) An insulated gate type semiconductor device according to claim 3 or 6, wherein the auxiliary trench section is structure in dot pattern, viewed from top side of the semiconductor substrate.

10.(Amended) An insulated gate type semiconductor device according to at least any one of claims 1 through 9,

wherein in a region around a cell region, there are arranged:

a terminal trench section filed with insulating material inside; and

a terminal floating region surrounded by the drift region, the terminal floating region having a first conductive type semiconductor, and

bottom of the terminal trench section is arranged in the terminal floating region, and

a space between adjoining terminal floating regions is narrower than a space between the bottom surface of the body region and a top of the terminal floating region.

11.(Amended) Manufacturing method of an insulated gate type semiconductor device which comprises: a body region arranged at upper surface side in a semiconductor substrate, the body region having a first conductive type semiconductor; a drift region being in contact with bottom surface of the body region, the drift region having a second conductive type semiconductor; a trench section arranged with penetrating the body region from upper surface of the semiconductor substrate and reaching level further below bottom surface of the body region; and a gate electrode arranged in the trench section with facing

the body region, the manufacturing method comprising:

trench section forming step of forming the trench section in the semiconductor substrate on which the drift region and the body regions have been formed;

oxide film forming step of forming an oxide film on a side wall of the trench section formed in the trench section forming step;

impurity injecting step of, after formation of the oxide film in the oxide film forming step, injecting impurity from bottom of a trench section formed in the trench section forming step;

insulating material laying-up step of laying up insulating material in the trench section after impurity is injected through the impurity injecting step; and

floating region forming step of forming a floating region by applying thermal diffusion processing after the insulating material is laid up in the insulating material laying-up step.

12. (Unchanged) Manufacturing method of an insulated gate type semiconductor device according to claim 11 further comprising:

trench section drilling step of further drilling down bottom of the trench section after impurity is injected in the impurity injecting step; and

impurity re-injecting step of re-injecting impurity from bottom the trench section drilled further in the trench section drilling step.

13. (Amended) Manufacturing method of an insulated gate type semiconductor device according to claim 11 or 12, wherein

the trench section is formed in a cell region and a region around the cell region in the trench section forming step, and

the insulating material laying-up step comprises:

insulating material filling step of filling inside of the trench section formed in the trench section forming step with insulating material; and

deposited material adjusting step of adjusting height of a deposited insulating layer by eliminating a portion of insulating material in the trench section filled with insulating material in the insulating material filling step, particularly, the trench section in the cell region.

14. (New) An insulated gate type semiconductor device according to claim 1 or 3, wherein

a thickness of the deposited insulating layer is a thickness enough to form peaks of electric field at two positions in a direction of thickness of the semiconductor substrate.

15. (New) An insulated gate type semiconductor device according to claim 6, wherein

a depth of the auxiliary trench section is a depth enough to form peaks of electric field at two positions in a direction of thickness of the semiconductor substrate.

16. (New) An insulated gate type semiconductor device according to any one of claims 1, 3, and 6, wherein

the lower end of the gate electrode and the bottom surface of the body region are substantially the same in depth.

17. (New) An insulated gate type semiconductor device according to any one of claims 1, 3, and 6, wherein

the floating region has a nearly circular shape in section.

18. (New) Manufacturing method of an insulated gate type semiconductor device according to claim 11 further comprising:

etching-back step of removing part of the insulating material by a depth substantially equal to the bottom surface of the body region after the insulating material is laid up in the insulating material laying-up step; and

gate material laying-up step of laying up a gate material in a space formed in the trench section in the etching-back step.